CLAIMS

1. An identification system comprising a reader including a transmitter for transmitting a signal and a plurality of transponders, each transponder including a receiver for receiving the reader signal and a transmitter for generating a response signal containing data which identifies the transponder, the transponder being adapted to repeat the transmission of the response signal at intervals which are random or pseudo-random in length, characterised by a counter driven by a clock, the output from the counter providing a random number or providing a seed value for a random number generator to affect the randomness of the intervals between the response signals.

2. An identification system as claimed in claim 1, wherein the counter and the clock are reset upon activation of a POWER-ON-RESET (POR) circuit.

3. An identification system as claimed in claim 1 or claim 2, wherein the counter and clock is part of an RFID chip.

4. A transponder comprising receiver means for receiving a reader signal, transmission means for transmitting a response signal containing data which identifies the transponder, the transponder being adapted to repeat the transmission of the response signal at intervals which are random or pseudo-random in length, characterised by a counter driven by a clock, the output from the counter providing a random number or providing a seed value for a random number generator to affect the randomness of the intervals between the response signals.

5. A transponder as claimed in claim 4, wherein the counter and the clock are reset upon activation of a POWER-ON-RESET (POR) circuit

6 An integrated circuit for use in a transponder, comprising receiver means for receiving a reader signal, transmission means for transmitting a response

signal containing data which identifies the transponder, the integrated circuit being adapted to repeat the transmission of the response signal at intervals which are random or pseudo-random in length, characterised by a counter driven by a clock, the output from the counter providing a random number or providing a seed value for a random number generator to affect the randomness of the intervals between the response signals.

7 An integrated circuit as claimed in claim 6, wherein the counter and the clock are reset upon activation of a POWER-ON-RESET (POR) circuit.

8 An integrated circuit as claimed in claim 7 or claim 8, wherein the integrated circuit is part of an RFID chip.

9 A method of identifying a plurality of transponders, comprising exposing a transponder to RF whereby a capacitor is charged to a predetermined value to activate a POWER-ON-RESET (POR) circuit, the transponder being responsive to a command signal from a reader to cause or repeat the transmission of a response signal, containing data which identifies the transponder, at intervals which are random or pseudo-random in length, characterised by a counter driven by a clock responsive to activation of the POR to provide an output signal when the command signal has been received, the output signal providing a random number or a seed for a random number generator, a slot selection or random transmit repeat (hold-off) value for the response signals being dependent directly or indirectly on said output signal.

10 An identification system as claimed in claim 1 or claim 2, wherein the counter and clock are routed to a latch such that when a command is received by the transponder, the instantaneous value of the counter is stored in the latch.

11 An identification system as claimed in claim 10, wherein the latch provides a random number or a seed value for a random number generator to affect the randomness of the intervals between the response signals.

12 A transponder as claimed in claims 4 or 5, wherein the counter and clock are routed to a latch such that when a command is received by the transponder, the instantaneous value of the counter is stored in the latch.

13. A transponder as claimed in claim 12, wherein the latch provides a random number or a seed value for a random number generator to affect the randomness of the intervals between the response signals.

14 An integrated circuit as claimed in claim 6 or 7, wherein the counter and clock are routed to a latch such that when a command is received by the transponder, the instantaneous value of the counter is stored in the latch.

15 An integrated circuit as claimed in claim 14, wherein the latch provides a random number or a seed value for a random number generator to affect the randomness of the intervals between the response signals.